Claims 12 to 23 (canceled)

Claim 24 (withdrawn) The transistor of claim 9 wherein said first source/drain region is a source region, said second source/drain region is a drain region and wherein said first V_T is higher than said second V_T.

Claim 25 (previously added) The transistor of claim 10 wherein said first source/drain region is a source region and said second source/drain region is a drain region.

Claim 26 (withdrawn) The transistor or claim 11 wherein said first source/drain region is a source region and said second source/drain region is a drain region.

REMARKS

Claim 10 has been amended, and claims 9, 11, 24 and 26 have been withdrawn from consideration. Accordingly, claims 10 and 25 are still active in this application. The amendment to claim 10 further clarifies the fact that all references to doped regions refer to portions of the channel.

Claim 10 and 25 were rejected under 35 U.S.C, first paragraph, as failing to comply with the written description requirement, the rejection alleging that claim 10 refers to the third embodiment and that the specification does not provide support for the claim language "said channel region having an implanted one of a positive of negative V_T dopant intermediated said source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent said source/drain regions, the opposite of said dopant in said channel region". This allegation is without merit as will be demonstrated and therefore respectfully traversed.

As stated at page 5, lines 9ff, "the FET can be made symmetrical rather than asymmetrical as described in the first and second embodiments with a different implant in the center of the channel region relative to the source and drain ends of the channel region. This means that the channel has a central portion different from the region of the channel adjacent both of the source/drain regions and is the same as the first or second embodiments except that the asymmetry has been changed to symmetry with respect to the regions 29 (Fig. 4B) as opposed to the region 17 (Fig. 1D) or region 23 (Fig. 2C). As stated at page 3, lines 13ff, "[t]he controlling region could have a positive V_T and the rest of the channel could have a negative V_T, ... The same applies for p-channel transistors except for a polarity reversal". It follows that either a positive or a negative implant can be used, depending upon whether n-channel or p-channel transistors are being fabricated as is also well known to even a pedestrian in the art. Also, with reference to Figs. 1A to 1D, it is stated at page 7, lines 4ff, "For an n-channel device (it is understood that all conductivity types will be opposite for a p-channel device),... This again demonstrates that both n-channel and p-channel devices are being covered by the language allegedly not supported by the specification. It is further stated at page 4, lines 15ff, "[i]t should be understood that the high V_T implant can be a counter doping of the low V_T implant with appropriate masking to perform the implants in this manner". Counter doping can only be provided by doping first with a first conductivity type dopant and then doping in the same region with a dopant of opposite conductivity. It follows that there is more than adequate support for the portion of claim 10 allegedly not supported by the disclosure.

Claims 10 and 25 were rejected under 35 U.S.C. 112, second paragraph, as being indefinite, the Examiner stating that it is not clear, in the clause in claim 10 discussed in connection with Issue 1. which portion of the channel region the phrase "said channel region" refer to: the region

intermediate the source/drain regions, or the regions adjacent the source/drain regions. The rejection is without merit and therefore respectfully traversed.

Claim 10 very clearly states that it includes "a channel region between said source/drain regions in said substrate". This means that the entire channel region is disposed between the source/drain regions as is standard in semiconductor technology. Claim 10 goes on to state "having a relatively low V_T central region between said source/drain regions and relatively high V_T regions adjacent to said source/drain regions". This very clearly means that the channel region has a relatively low V_T region in the central portion of the channel which is redundantly stated to be between the source/drain regions and relatively high V_T regions adjacent to the source/drain regions, or, otherwise stated, between the central region and the source/drains. This language is clear and unambiguous.

Claim 10 was rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (U.S. 4,371,955 B1). The rejection is respectfully traversed.

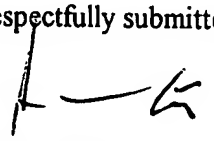
Claim 10 requires, among other features, a channel region between the source/drain regions in the substrate having a relatively low V_T central region between the source/drain regions and relatively high V_T regions adjacent to the source/drain regions, the channel region having an implanted one of a positive or negative V_T dopant intermediate the source/drain regions and having an implanted one of a negative or positive V_T dopant adjacent the source/drain regions, the opposite of the dopant in the central region as discussed above. This claim refers to the fourth embodiment as discussed on pages 5 and 9 of the specification. No such features are taught or suggested by Sasaki either alone or in the total combination as claimed.

A review of Sasaki at column 3, lines 16ff indicates that the semiconductor layer 21 is p-type (line 18) and boron, which is a p-type dopant, is implanted into the regions 211b' and 211c' (line 23). It follows that the regions 211a, 211b and 211c are all p-type with differing doping levels. This is not a dopant of opposite conductivity type in the central region of the channel relative to the dopant in the regions of the channel adjacent the source/drain regions as claimed. It follows that claims 10 defines patentably over Sasaki under either 35 U.S.C. 102 or 103.

Claim 25 depends from claim 10 and therefore defines patentably over Sasaki for at least the reasons set forth as to claim 10.

In view of the above remarks, favorable reconsideration and allowance are respectfully requested.

Respectfully submitted,



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